intel®

8244

GAME CHIP

for

MAGNAVOX

The 8244 is a general purpose graphics display device that operates in conjunction with raster scan type displays. Its primary purpose is to provide a means for generating and moving objects on a TV screen for use in the consumer game market. However, its generality and flexibility makes it suitable for use also in teaching machines, animation displays, simulation trainees, and etc.

This device is a peripheral that communicates over the data and address bus of the 8048/8748. Although other microprocessors may be used with it, these particular devices provide the greatest capability for the low system cost.

FEATURES

- Single 5V supply
- 28 pin CerDip or plastic DIP package.
- 8048/8748 / 8085 Compatible.
- Complete NTSC color TV sync generator.
- Provides shapes that are mask programmable into internal ROM.
- Accommodate up to 32 object locations on the display simultaneously.
- Devices may be multiplexed to provide greater than 32 object locations on the displ
- All movement of objects displayed is under software control in the microprocessor.
- Display objects that collide return status and location information to the microprocessor.
- Provides Red, Green, Blue, Luminance, and Sound outputs.

over full commercial specification of temp. when both chips are exposed to same envir
except not interlace

*Note: Signals that are asserted when the variable is low voltage are designated by a —. eg. $\overline{CS}$ is active low.

SYMBOL	I/O	PIN NUMBER	
D0 - D7	I/O	TBD	Data/Address lines to/from 8048/8748.
$\overline{CS}$	I	TBD	Chip Select enables writing to or reading from the addressed functional block within the device
ALE	I	TBD	Address Latch Enable allows the contents of the multiplexed address/data bus to be interpreted as an address.
$\overline{WR}$	I	TBD	Write Strobe causes the bus data to be written into the previously selected memory element.
$\overline{RD}$	I	TBD	Read Strobe allows status and counter information to be read from the device.
$\overline{INTR}$	O	TBD	Interrupt request to the microprocessor, set Low for request and cleared when the status register is read.
CSY	O	TBD	Composite sync contains horizontal sync, serrated vertical sy and equalizing pulses.
VBL	I/O	TBD	Vertical blanking identifies the period during which the display is blank while the CRT beam is in vertical retrace.
HBL	I/O	TBD	Horizontal blanking identifies the period during which the display is blank while the CRT beam is in horizontal retrace.
M/S	I	TBD	Master/Slave designates a device to be either a master or a slave unit. A master, so designated, feeds VBL and HBL to itself from its internal sync generator and also sends VBL an HBL out to the slave device if one exists. A slave, so

can be "ored" Treable

If external, must be sync to 3.58 clock

The duty cycle shall be 50% with <5% deviat

designated receives VBL and HBL for its internal synchronization.

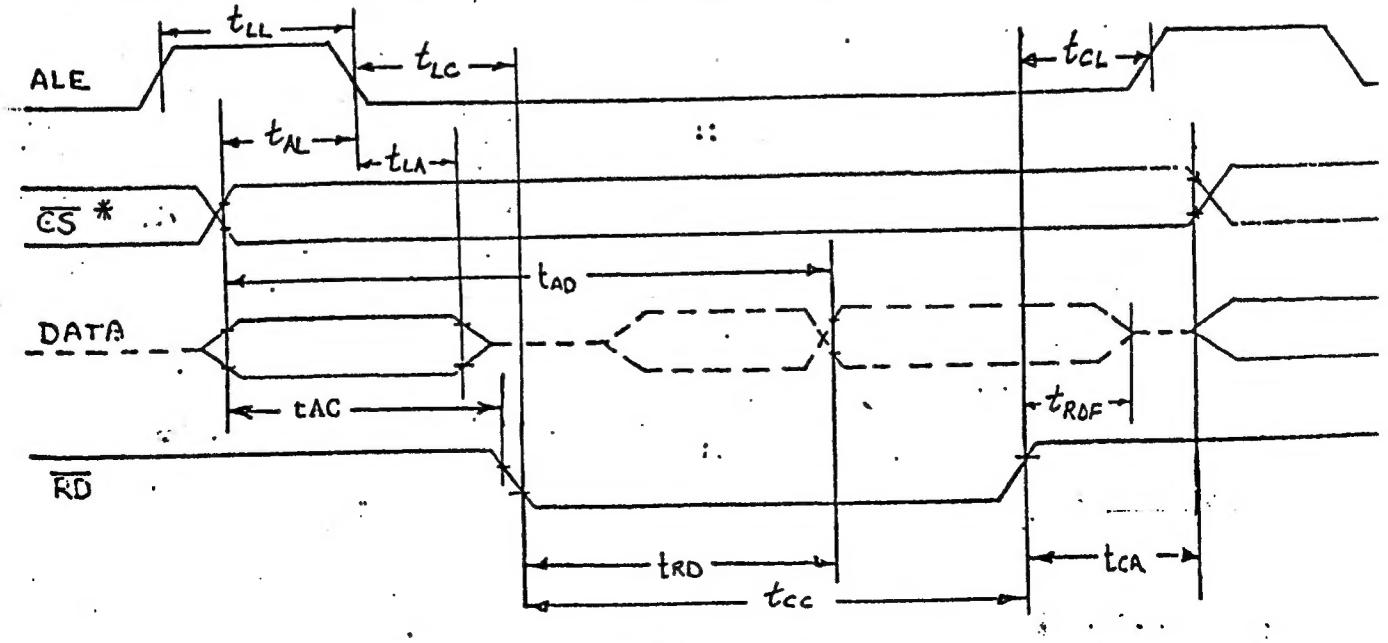
CLK	I	TBD	The clock input operates at a fixed frequency of 3.58 Mhz.
R	O	TBD	The Red output is a chroma signal representing objects that are to be displayed in a red color.
G	O	TBD	The Green output is a chroma signal representing objects tha are to be displayed in a green color.
B	O	TBD	The Blue output is a chroma signal representing objects that are to be displayed in a blue color.
L	O	TBD	The Luminance output represents the ORed result of active patterns in the minor system, the major system, and the grid (if set grid bright is active).
BG	O	TBD	The Burst Gate defines the duration of the 3.58Mhz color reference signal required for generation of the composite co signal in external analog circuitry.
SND	O	TBD	The Sound output provides an audio driving signal to the external sound modulator.
STB	I	TBD	The position strobe input.
CX	I	TBD	Chip Expander. If there are 2 8244's in a system, L is connected to CX#1 and Lum#1 connected to CX#2. This allows statu
VCC	I	TBD	+5V supply
VSS	I	TBD	Gnd.

References: "Standard Peripheral Timing for 8085 Bus", April 20, 1976 8048/8748/8035 preliminary data sheet, September 1976. overlaps between objects on differe chips to be read by the CPU.

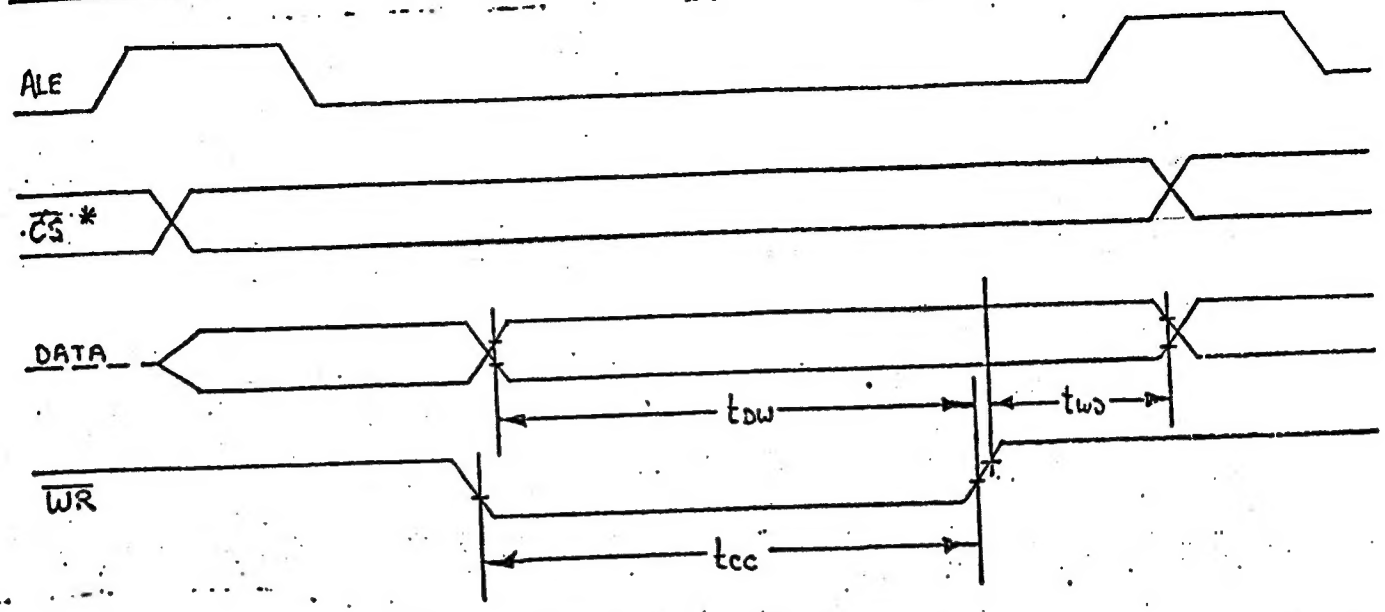
SUMMARY

The 8085 timings are more restrictive than the 8048 timings. Although the initial game product will match an 8244 with an 8048 it is desirable to design the 8244 to work with both the 8048 and the 8085. This will allow upwards compatibility with the more powerful CPU and very probably will extend the product life of the 8244. The following timings should allow the 8244 to work in either system.

READ CYCLE:



WRITE CYCLE:



* Assumes the 8244 chip select input comes from a high order address bit.

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
tAL	Address valid before T.E. of ALE	50		NSEC
tLA	Address hold time after ALE	100		NSEC
tLL	ALE width	100		NSEC
tAC	Address valid to L.E. of control	150		NSEC
tLC	T.E. of ALE to L.E. of control	100		NSEC
tAD	Address valid to valid data out		400	NSEC
tRD	Data out delay from RD		150	NSEC
tRDF	Data bus float after RD	10	75	NSEC
tCC	Width of control	250		NSEC
t_{DW}	Data in valid to T.E. of WR	150		NSEC
tWD	Data valid after T.E. of WR	0		NSEC
tCL	T.E. of control to L.E. of ALE	20		NSEC
tRV	T.E. of control to L.E. of next control	300		NSEC
tCA	Address hold after control	0		NSEC

NOTE: The 8244 will ignore the information on the data lines except for the cycl
when $\overline{RD}$ or $\overline{WR}$ are active.

R,G,B + L must come out within a 25 nsec. time per

8244 ELECTRICAL SPECIFICATION

D.C. CHARACTERISTICS

$T_A = 0^oC$ to ~~55°C~~ 70°C; $V_{CC} = +5V \pm 5\%$; $V_{SS} = 0V$

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_{IL}	Input low voltage	V_{SS}-.5		0.8	V	
V_{IH}	Input high voltage	2.0		V_{CC}	V	
V_{OL}	Output low voltage			0.45	V	I_{OL} = 1.6mA
V_{OH}	Output high voltage	2.4			V	I_{OH} = -200μA
I_{IL}	Input leakage			±20	μA	$(V_{SS} + 0.45) \leq V_{IN} \leq V_{CC}$
I_{CC}	V_{CC} current drain			200	mA	

A.C. CHARACTERISTICS

$T_A = 0^oC$ to 55^oC; $V_{CC} = 5 \pm 5\%$; $V_{SS} = 0V$

Timing measurements are made at the following reference voltages unless otherwise noted:

Input "1" = 2.0V, "0" = 0.8V
Output "1" = 2.0V, "0" = 0.8V

Output loading consists of one TTL load and 50pf total external capacitance except the system bus which is loaded by one TTL load and 100pf.

Rise and fall times worst case will be .200 ns less. Rise and fall times will be measured from 10% and 90%.

Functional Specification

The 8244 is organized as a group of subfunction blocks that communicate via an internal bus with the I/O port Most of the subfunctions are individually addressable for the transfer of information with the controlling microprocessor. These blocks may be categorized functionally as follows:

1. Major display system
2. Minor display system
3. Grid display system
4. Sound system
5. Status and control circuits
6. Sync generator

The use of both major and minor display systems provides hardware parallelism to circumvent the problem of concurrent objects. In general, the single major system is used to display fixed objects, while the plurality of minor systems similarly handles moving objects. In exceptional cases nonstrategic moving objects may be placed in the major system but this should be avoided where accommodation is provided by the minor systems. All objects in the major system are composed of 3 x 7 bit arrays,* while all objects in the minor system are composed of 8 x 8 bit arrays. Larger objects are produced by concatenation of the basic arrays. All major system objects start on even lines.

The grid display system places a segment programmable grid in the background of the display. An grid segment may be either inserted or deleted programmatically to produce a variety of arrays such as checkerboards, racetracks, mazes, and etc. An additional feature allows vertical segments to be expanded horizontally and thus provide illuminated square and rectangular areas.

The sound system contains both a random noise generator as well as a programmed sound section. The resulting signals may be combined digitally to produce special effects such as gun shot sounds.

The status and control circuits provide a message transfer mechanism between the 8244 and the microprocessor. Control messages sent from the microprocessor are utilized within the control circuits. These messages determine the types of status messages to be returned and also define certain key conditions associated with the displayed objects. The status messages returned to the microprocessor from the 8244 provide information relative to the display that is used by the microprocessor for input to the program.

* An 8x7 array is composed of 8 horiz dots and (7x2) horiz l

The sync generator provides both sync and blanking signals for use internally on the chip as well as an output for use by the accompanying TV modulator circuitry. A color burst gate is also provided as an output for use by the modulator. The manner in which the sync generator output signals are utilized is determined by the programming of the M/S input pin. A high level of '1' input designates the Master mode and causes the sync generator outputs to drive both internal circuitry and to provide outputs on the appropriate pins (HBL, VBL, CSY, and BG). Conversely, a low level or '0' input designates the Slave mode and allows the HBL and VBL pins to be used as inputs which are then driven by another 8244 designated as a Master. In this latter case, both CSY and BG are derived from the Master 8244 along with HBL and VBL for use by the external circuitry. A non interlaced sweep format is used, primarily, to eliminate the objectionable effect known as "color crawl". The resulting sweep rates are close to American NTSC standards so that there will be no difficulty in synchronization. For operation on European standards, the 8244 will be operated in the Slave mode and appropriate signals will be supplied to it from external sync circuitry.

Major Display System

The purpose of the major display system is to position and select both specific fixed objects and also non-colliding moving objects of a non-strategic nature. This system can position a total of 28 objects in the static positioning mode[1] and a greater number in the dynamic positioning mode[2]. The positioning of each individual object requires 15 bits of addressing information. All addressing is physically relative to the upper left hand corner of the display field. The first 7 bits specify the vertical position which can be on one of 121 scanning lines in a field. The remaining 8 bits specify one of 183 positions horizontally across the screen. All objects in the major system are fixed in size, whereas, the minor system objects may be doubled in both dimensions programatically.

The major system is partitioned into a pair of groups, where each group is optimized for different types of displays. This expedient allows a considerable reduction in chip size without adversely affecting total function. Primarily, the first group provides for alphanumeric or grouped object display by allowing each CAM location to point to a character group of up to four arbitrarily selectable objects. These objects have a fixed spacing of 16 clock intervals which allows matching of object placement with the grid format. Thus, a single CAM location may place up to four objects centered within the grid areas. For the purpose of textual presentation,

[1]The static positioning mode loads all object data during the vertical blanking interval.

[2]The dynamic positioning mode loads any or all object data during the horizontal blanking interval.

associated pairs of CAM locations may locate alphanumerics in an interspersed fashion so as to provide adjacent characters. Alternatively, any object spacing may be achieved either by programming appropriate blanks or different starting locations.

Address starts @ 40H

The first group uses four CAM locations to provide starting points for multiple objects. Each CAM location ~~contains two "don't care" bits in its horizontal section and thereby~~ is able to point to four LSS* locations. Thus, the first group controls the placement and selection of 16 objects. If any patterns are truncated all four grouped objects will be shortened by the amount of the shortest object.

Address starts @ 10H

The second group within the major system provides for the placement of game obstacles that are either fixed in location or may be movable within certain restrictions. As movable objects, they should not be utilized as strategic elements such as balls, bullets, race cars, etc. However, they do provide slow moving obstacles such as covered wagons or other vehicles. In addition, these objects, when moving, should be prevented from overlapping any other objects in the major system as no means for identification by the microprocessor is available. This nonoverlapping function is achieved by proper programming. Within this group there is a one to one correspondence between a CAM location and a single displayed object. Since there are 12 CAM locations in the second group, there are also 12 objects that may be placed.

The portion of the total CAM array that constitutes the major system points to a total of 28 storage locations in the LSS. The information stored in the LSS represents the location address of the associated pattern in the pattern ROM. Rather than store the starting address of the desired pattern in the LSS, a two's complement displacement is stored. This expedient allows a simple hardware mechanism for sequencing through the consecutive addresses of ROM patterns as they are encountered. The displacement represents the difference between the starting address of the object pattern in ROM and the scanning line number in the raster display. This may be simply stated as follows: (Vertical Pos.)/2 See memory map

(LSS) = Object Starting Address - Hor. Scan Line Number

A single 9 bit adder is sufficient for accommodating all address sequencing for the major system. The LSS must be able to store 9 bit displacements. The sequence of events that takes place for the placement of an object pattern is as follows: As a match occurs between the contents of the beam location counter and the address stored in any particular CAM cell, a pointer enables an output from the particular associated LSS location. This output displacement quantity is added to the scan line number, obtained from the line counter, and results in the address of the desired row of the object pattern in ROM. If the full 8x7 pattern

*LSS= Linear Select Store

is desired, then the first match of the CAM causes the above described procedure to produce the starting address of the object pattern in ROM. As horizontal matches occur on successive scan lines, a consequential incrementation of the ROM address occurs. An end of pattern address is detected on every eighth address and terminates the presentation of each particular object. There is no restriction as to whether a full 8x7 or any portion of the pattern in the vertical dimension may be presented as a displayed object. This flexibility allows the programmer to use fractions of object patterns if it is expedient to do so.

In addition to the 9 bit displacement in each location in the LSS, there is provision for the storage of 3 color bits. These bits designate the primary colors red, green, and blue. By the activation of more than one color bit simultaneously, various hues are also produced.

The following table presents a summary of the specifications for the major system:

Group	No. of CAM Loc.	No. of Bits in Vert. CAM	No. of Bits in Hor. CAM	No. of Simul. Objects CAM Loc.	No. of Simul. Objects Group	No. of Selectable Objects	Disp. Bits in LSS	Attribute Bits in LSS	Object Size
1	4	7	~~6~~ 8	4	16	64 ~~45~~*	9	3	8 dots wide 14 ~~inches~~ lines high
2	12	7	8	1	12	64 ~~45~~*	9	3	8 dots wide 14 lines high

*There are 64 ~~45~~ objects total, any of which can be selected by either Group.

Major systems can be stacked with no blank lines between them

SYNC GENERATOR

The sync generator operates as a non-addressable autonomous circuit block within the 8244. As such, it provides a source for synchronizing signals both for internal use by the 8244 circuitry and for transmission to external circuitry. Externally the signal becomes processed with the color, luminance, and sound signals and ultimately results in synchronization of the associated TV receiver.

The manner in which the signals are utilized is determined by the mode in which the 8244 operates in a particular configuration. In a small system, utilizing a single 8244, it is operated in the Master Mode by connecting the M/S pin to Vcc. The resulting signals from the sync generator then drive both the display circuitry on the 8244 and also exit the chip, via appropriate pins, to drive the external circuitry.

In larger system configurations, where the need for more than one 8244 exists, a single 8244 is designated the Master, as previously described. In addition, one or more 8244's become Slave Mode devices by connecting their M/S pins to Vss. The sync generator on a Slave Mode device is free to run but the output is not utilized.

In Master Mode operation the sync generator signals used internally by the 8244 are horizontal blanking (HBL) and vertical blanking (VBL). Correspondingly, these two signals provide outputs along with composite sync (CSY) and color burst gate (BG). In Slave Mode operation the 8244 receives only HBL and VBL from a Master Mode 8244. For operation on European TV standards, the 8244 is placed in the Slave Mode. It then receives HBL and VBL from an external sync signal source such as an LSI device or appropriate discrete circuitry.

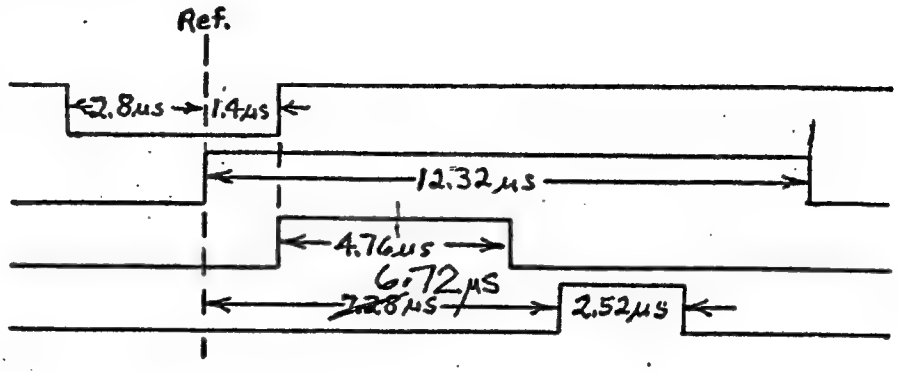
The sync generator provides non-interlaced synchronizing signals. It operates from the basic color subcarrier frequency of 3.58 Mhz. This clocking signal is divided by a factor of 227.5 in order to obtain the horizontal line frequency of 15,734.3Hz.

The horizontal line frequency is divided by a factor of 263 to produce the vertical sync frequency of 59.83Hz. In the following timing diagrams, those signals shown under Horizontal Timing are reproduced at the 15,734.3Hz rate, while the signals shown under Vertical Timing are reproduced at the 59.83Hz rate. In addition, certain signals generated at the horizontal frequency are enabled only during portions of the vertical interval. In particular, the serrated portion of the vertical serration sync pulse is shown under Serrated Pulse. It is generated at the 15,734Hz rate and is gated on for three pulse duration intervals at the 59.83Hz rate. This may be observed under Vertical Timing in the Composite Sync waveform. In this

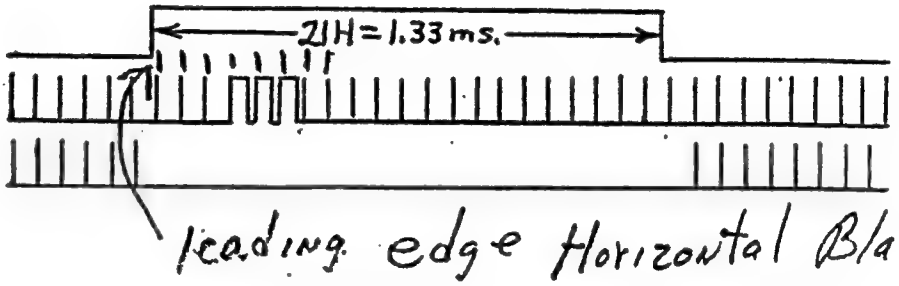
SYNC GENERATOR

signal horizontal sync is ORED with the gated vertical serration sync pulse. Similarly, the burst gate is generated at the 15,734Hz rate, but is inhibited at the 59.83Hz rate during the vertical blanking interval.

HORIZONTAL TIMING



VLRTICAL TIMING



leading edge Horizontal Blan

MINOR DISPLAY SYSTEM

As a first order objective all strategic objects are selected and displayed by the minor display system. In some games it may be useful to put fixed objects in the minor system and there is no restriction that prevents this. There are four replicated blocks within the minor system. Each block is autonomous in function and provides for the placement of a single object. Each of these objects may collide with each other or with objects in the major system. In either event, the minor object is readily identifiable by the microprocessor so that immediate responsive action may be taken.

Minor system objects are locatable by a portion of the overall CAM array, just as in the major system. However, the similarity of the two systems ends in the signal path beyond the CAM array. Each of the four CAM locations in the minor system is dedicated and points to a singular block of object pattern bits located in RAM storage. In contrast, the CAM locations in the major system can point to any 64 of the 45 objects stored in the pattern ROM. In addition, the mechanism for sequencing through the rows of the pattern RAM's is different than that used in the major system. In place of a singular adder as used in the major system, each minor system contains its individual three bit counter. This counter is updated at the beginning of each horizontal scan line. The decoding of the counter points to the proper location in the pattern RAM. Thus, each dot row in an object is presented as the RAM locations are sequenced. The RAM locations are loadable from the internal bus by a Write operation of the microprocessor. The RAM has the capacity to store eight bytes for each object thereby allowing an 8 x 8 object presentatic Associated with each minor system is an Attribute Register whose contents are arranged as follows:

7	6	5	4	3	2	1	0
X	X	B	G	R	D	S	X_9

The Bits in this register are defined as follows:

Bit 0 - X_9 is the ninth Bit in the horizontal address of the beam location. This bit allows the beam location to be resolved to 140ns increments.

Bit 1.- The S or smoothing Bit allows a displacement of either the odd or even count horizontal sweep lines in order to provide an improved appearance of objects that visually rotate on the screen.

Bit 2 - The D or duration Bit determines whether an object will be presented in normal size or if its x any y dimensions will be increased by a factor of two.

Bit 3 - The R Bit specifies whether the object contains a red component of color display.

MINOR DISPLAY SYSTEM

Bit 4 - The G Bit specifies whether the object contains a green component of color display.

Bit 5 - The B Bit specifies whether the object contains a blue component of color display.

Bits 6 and 7 - These bits are unspecified and exert no control.

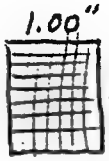
The definition of the delay of dot rows within an object depends on Bits 0, 1, and 2 as shown in the following table:

Bit 2 D	Bit 1 S	Bit 0 X_9	Even Line Delay (ns)	Odd Line Delay (ns)
0	0	0	0	0
0	0	1	140	140
0	1	0	140	0
0	1	1	0	140
1	0	0	0	0
1	0	1	280	280
1	1	0	280	0
1	1	1	0	280

Minor { 3.58 MHz ⇒ 280 nS period
0.125 inch on 25" tube
9th Bit → 0.0625 inch placement accuracy
X pos.

Major Placement Accuracy is 280ns ⇒ 0.125 X pos.

Horz Line seperation ≈ 0.070 inch on 25" screen



each dot will be 2 Horz Line.
Horz width of dot ≈ 0.125 inch
Vert height of dot ≈ 0.140 inch

Character (8X8) = (8x.14) x (8x.125) =

GRID DISPLAY SYSTEM

The grid display consists of an array of nine enclosed areas horizontally and eight areas vertically. Each line segment between the nodes of the array is individually controllable so that it may be presented or be inhibited.

A full array, consisting of all segments present, is created by combining nine complete horizontal display bars with ten complete vertical display bars. Each horizontal bar consists of nine concatenated bar segments, while a vertical bar consists of eight concatenated bar segments. Each horizontal bar on the TV screen is composed of three consecutive horizontal scan lines, while adjacent bars are spaced by 21 horizontal scan lines. A vertical bar is made up of a column of dot groups. Each dot group is programmable to consist of either two or sixteen clock intervals (3.58Mhz) in width*. A conventional grid utilizes two clock intervals while large area block arrays, such as checkerboards, utilize sixteen clock intervals. The spacing between adjacent vertical bars is ~~thirteen~~ fourteen clock intervals. Thus, wide vertical bar segments that are adjacent, appear to be continuous displayed areas. The grid is centered vertically on the TV screen by allowing the first or top horizontal bar to start on the 24th horizontal scan line relative to the end of vertical blanking (VBL). Similarly, horizontal centering is accomplished by allowing the first or left-most vertical bar to start on the 19th clock cycle from the end of hori:ontal blanking (HBL). ?

A programmable feature allows the grid to be ~~converted into~~ augmented by the addition a dot matrix. In this case the dots appear at a physical placement on the TV screen, where otherwise the intersection of the horizontal and vertical bars would appear. ~~The dots are electrically created by ANDing the electrical signals representing complete horizontal bars with the complete vertical bars.~~ ~~Thus~~ The dots are composed of three horizontal scan line segments that have ~~been shortened to~~ a width equivalent to two clock cycles. Since, a full array of dots is always presented, no segment programming requirement exists for dot arrays, although segments and dots can simultaneously be displayed.

An additional programmable feature allows the grid display, or any of its previously described subsets, to be either presented or inhibited on the TV screen.

The upper left hand corner of the grid has coordinates

~~(Y, X) = (18, 19)~~

X = 19 clocks from ~~[illegible]~~ lagging edge of Horizontal Blanking

Y = 18 lines from ~~top of screen~~ lagging edge of vertical blanking

*Horizontal displacement on the TV screen is directly proportional no time.

SOUND SYSTEM

The sound system generates a duty cycle modulated square wave from which an audio signal is extracted by means of an external low pass filter. The control of the duty cycle is effected by information that is transferred from the microprocessor to the 8244. This information consists of triple byte groups that determine the audio frequency and an accompanying 4 bits that determine volume.

The triple byte groups are loaded into three-eight bit shift registers located on the 8244. Each byte in the group is loaded sequentially into its respective register during a load interval. All three bytes are loaded in between consecutive shift clock pulses. The concatenat of the three registers results in a 24 bit string that is shifted out by this shift clock. The resulting serial pattern of ones and zeroes contains a fundamental band of frequency components that lie in the audio range. This particular signal is further "chopped" by a higher frequency that is a multiple of the shift clock. By duty cycle modulation of this "chopping" signal, the amplitude of the audio component is varied. There are four control bits that are used to control the audio level. These bits are loaded into a four bit down counter that is shifted by the high frequency shift clock. The resulting output is ANDED with the output from the three concatenated shift registers to produce the composite audio output. In addition to the four volume control bits, three other control bits are used to augment the overall operation of the sound system. A noise enable bit enablesa feedback path in the output eight bit shift regist in the 24 bit shift path to produce the noise conponent. Simultaneous the noise is added to the audio component that is progressing down the shift register.

The shift frequency for the 24 bit shift may be varied between two values by another control bit. This expedient allows low audio frequencies to be produced with fewer refresh cycles from the microprocessor than for high frequencies thus, reducing the load on the processor.

For the reproduction of certain audio tones that are subharmonically related to the shift clock, the need for microprocessor refresh is totally eliminated by recirculation of the 24 bit shift path. This recirculation path is activated by another bit in the sound control word. Under the recirculation mode of operation, the sound interrupt should be inhibited.

The format of the sound control word is described below:

7	6	5	4	3	2	1	0
8	R	S	N	V_3	V_2	V_1	V_0

LSB of Volume

Bits 0 - 3 - Volume Bits, collectively as a 4 bit word, these bits define the output audio level.

Bit - 4 - Noise Enable; controls noise generation and mixing with the audio signal. Bit 4 = 1, noise on; Bit 4 = 0, noise off.

shift freq
≈ 4KHz or 1KHz

SOUND SYSTEM

Bit 5 - Shift Frequency; determines frequency of shift clock. Bit 5 = 1, f = 3933Hz. Bit 5 = 0, f = 983Hz.

($3933Hz = \frac{H}{4} = \frac{15,734}{4}$; $983Hz = \frac{H}{16} = \frac{15,734}{16}$)

pure tones ≈ 100 Hz to 2KHz

Bit 6 - Recirculation Bit; determines closure of recirculation path around the 24 Bit shift path. Bit 6 = 1, recirculation active. Bit 6 = 0, no recirculation.

Bit 7 - ENABLE SOUND 0 = NO SOUND 1 = SOUND

For those modes of operation requiring sound refresh data from the microprocessor, an interrupt is generated each time that the 24 sound bits have been shifted through the three eight Bit shift registers. A 5 bit counter set to modulo 24 counts shift clocks and determines when the interrupt should occur.

The sound shift registers, volume counter and sound control word register are all individually addressed by the microprocessor for the purpose of loading data. The address of these elements is shown under the topic of "Address Structure."

Sound Interrupt will not be disabled during recirculate.

CONTROL AND STATUS

A0H

The control over various operational parameters on the chip is effected by the bits in the control word that is written into the control register by the microprocessor. The bits in the control word are defined as follows:

A0H

Bit 0 - Enable Horizontal Interrupt, generates an interrupt 20 us in advance of the occurrence of horizontal blanking. This advance notice to the microprocessor allows a sufficient interval for the reading of the status information so that appropriate control can be exerted during the horizontal blanking interval.

Bit 1* - Forced Position Strobe, allows the freezing of the beam location information in the X-Y position registers so that the microprocessor can locate the beam at any time. Bit 1 = 1 strobes beam location to X-Y registers. Bit 1 = 0 disables strobe internal, but external strobe through position strobe Pin can still take place.

Bit 2 - Enable Sound Interrupt, allows an interrupt to be generated whenever the sound register needs new data. Bit 2 = 1 enables sound interrupt, Bit 2=0 disables sound interrupt.

Bit 3 - Set ~~Grid Bright~~ Enable Grid, allows two luminance levels of the grid. If the bit is a 0, the luminance signal is inhibited during grid information intervals. If the Bit is a 1, the luminance signal is active during grid information intervals.

Bit 4 - Enable External Overlap, allows the detection of overlap, when more than one 8244 exists in a system. Objects that overlap or collide and exist in separate chips are enabled by this Bit. Bit 4 = 1 enables external overlap, bit 4 = 0 disables external overlap

Bit 5 - Enable Display, allows ~~turning on and off of the output color & luminance signals.~~ objects and grid to be displayed Bit 5=1 enables display; Bit 5=0 disables ~~all~~ outputs. The purpose of this bit is to allow the µP to write new data to the 824 when the display is part way through a display field. It is the responsibility the software to disable the display only when there are no active patterns being displayed

Bit 6 - Dot Enable, allows the presentation of a dot array in place of the grid array. The dots appear at the intersection of the horizontal and vertical lines in the grid format. Bit 6 = 1 enables dots; bit 6 = 0 enables normal grid.

Bit 7 - Grid Segment Width, allows the selection of narrow or wide vertical segments in the grid. Bit 7 = 1 enables wide segments; bit 7 = 0 enables narrow grid.

A3H WRITE ONLY ~~A3H~~ ~~Set Grid Bright~~

The color of the grid and background is determined ~~by~~ the data stored in the Color Latch. Also by setting the Enable Grid bit to '0' the grid can be turned off and the grid RAM can be used for other data storage. The bits in the Color Latch are defined as follows:

Bit 0 - Grid Color Blue
Bit 1 - Grid Color Green
Bit 2 - Grid Color Red
Bit 3 - Background Color Blue
Bit 4 - Background Color Green
Bit 5 - Background color Red
Bit 6 - ~~Enable Grid~~ Set Grid Bright

BLC - Beam Location C

This str. will not cause Sake data to be loaded into latch

* The "OR" of STB and Force Position Strobe will cause X-Y reg to follow the BLC. A falling edge on the OR output will freeze BLC. The reg will remain frozen until after the X-register is re

CONTROL AND STATUS

A2H WRITE ONLY

The Enable Overlap register allows for selectable masking of overlaps. When a bit in the Enable Overlap register is a '0' the overlap of that object with any other object will not set the bits for the other objects in the Overlap Status register. The bit pattern is as follows:

Bit 0 - Minor System 0
Bit 1 - Minor System 1
Bit 2 - Minor System 2
Bit 3 - Minor System 3
Bit 4 - Vertical Grid
Bit 5 - Horizontal Grid and dots
Bit 6 - External Chip
Bit 7 - Major System

* A2H ~~A2H~~ READ ONLY

The Overlap Status register stores the coincidences of intensified bits as they occur on the screen. Whenever two or more objects are simultaneously displayed the bits for both objects are set unless the Enable Overlap register has those bits masked. The External Chip overlap corresponds to the Signal on the 'CX' Pin. The bit pattern is the same as that of the Enable Overlap Register above.

A1H Read ONLY one once per cycle I THINK ! MUST STAY FROM EXECUTIVE

The Control Status word is used to determine the chip status and interrupt sources. The bit pattern is as follows:

Bit 0 - Horizontal Status - Starts 20 us before Horizontal blank starts Ends 5 us before Horizontal blank ends.

Bit 1 - Position Strobe Status-Status of X-Y Register strobe '1' = Follow Beam Location Ctr, '0' = latched. (See note on page 14)

Bit 2 - Sound Needs Service - Sound register empty

Bit 3 - Vertical Status = Vertical Blanking

Bit 4 - N/C

Bit 5 - N/C

Bit 6 - External Chip Overlap - Set when an overlap occurs with signal on 'CX' Pin.

Bit 7 - Major System Overlap - Set when the chip attempts to ~~display two major system patterns simultaneously~~ load maj System shift register if shift register all ready has a one.

The status register bits 2,6 and the interrupt flip flop are cleared by reading the status reg.

* The overlap status register is cleared when read.

ADDRESS STRUCTURE

The subfunction blocks within the 8244 may be individually addressed for the writing and in some cases, the reading of data. The addressing structure of these blocks is shown below:

CAM AND LINEAR SELECT STORE

ADDRESS	SUBFUNCTION
Bit: 7 6 5 4 3 2 1 0	
0 0 0 0 ← Object Number → 0 0	LINE CAM
0 0 0 0 ← Object Number → 0 1	DOT CAM
0 0 0 0 ← Object Number → 1 0	LSS BITS 0-7
0 0 0 0 ← Object Number → 1 1	LSS BITS 8-11

Note: For the Minor System LSS Bits 0-7 are attribute bits stored in the Attribute register.

MINOR SYSTEM PATTERN RAM

ADDRESS	SUBFUNCTION
Bit: 7 6 5 4 3 2 1 0	PATTERN RAM
1 0 0 ← OBJECT NUMBER; PATTERN RAM LINE NUMBER →	

MISCELLANEOUS REGISTERS

ADDRESS	SUBFUNCTION
Bit: 7 6 5 4 3 2 1 0	
1 0 1 X 0 0 0 0	CONTROL
1 0 1 X 0 0 0 1	CONTROL STATUS
1 0 1 X 0 0 1 0	OVERLAP STATUS AND ENABLE OVER
1 0 1 X 0 0 1 1	Y REGISTER
1 0 1 X 0 1 0 0	X REGISTER
1 0 1 X 0 1 0 1	N/A
1 0 1 X 0 1 1 0	SOUND 0
1 0 1 X 0 1 1 1	SOUND 1
1 0 1 X 1 0 0 0	SOUND 1
1 0 1 X 1 0 0 1	SOUND VOLUME
1 0 1 X 1 0 1 0	

ADDRESS STRUCTURE

GRID

ADDRESS								SUBFUNCTION
Bit:	7	6	5	4	3	2	1	0	
	1	1	0	COLUMN →				0	HORIZONTAL SEGMENTS 0 t
	1	1	0	NUMBER				1	HORIZONTAL SEGMENTS 8
	1	1	1					0	VERTICAL SEGMENTS

READ & WRITE CAPABILITY:

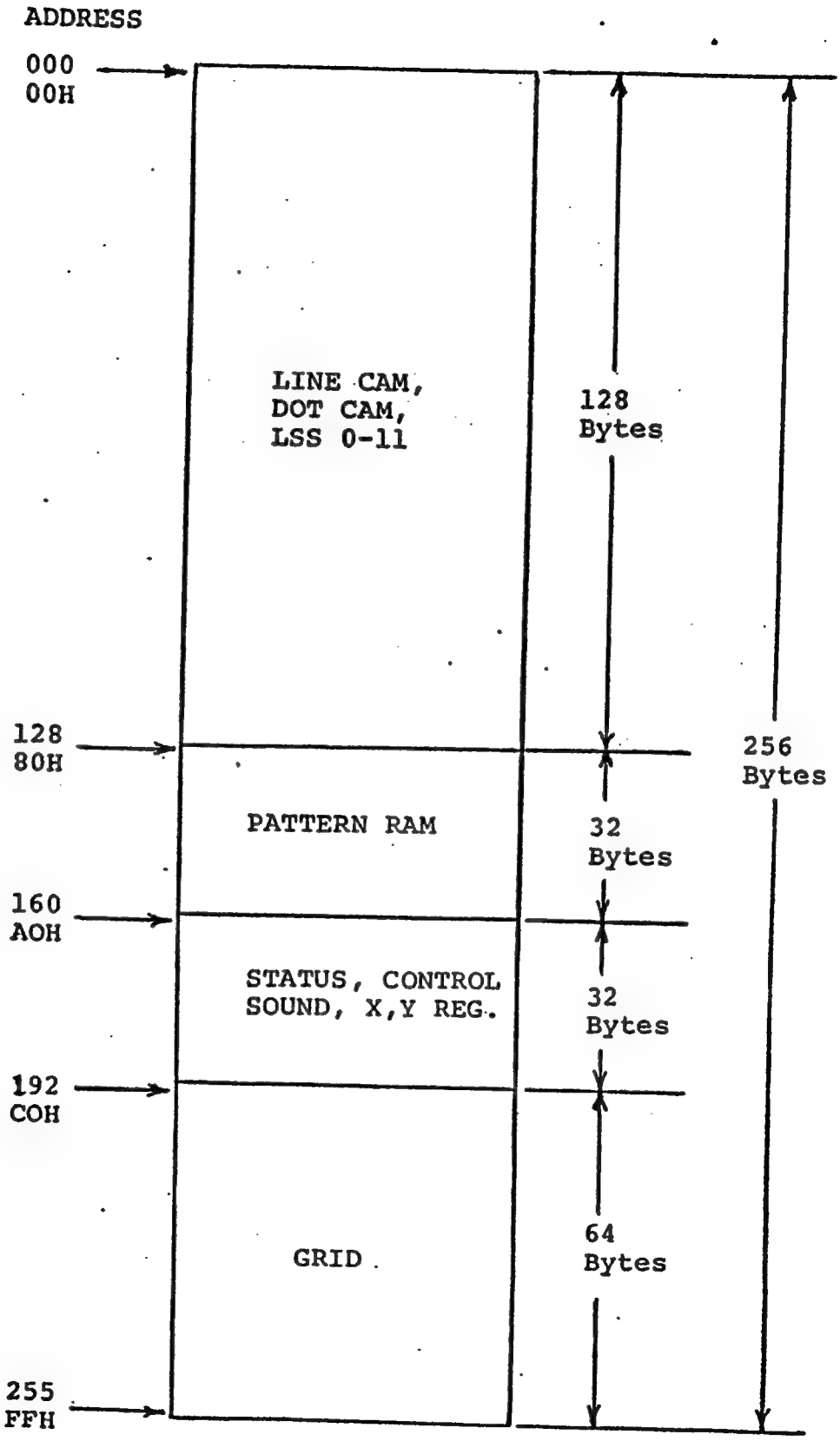
READ/WRITE:
- ALL CAM
- ALL LINEAR STORE EXCEPT MINOR SYSTEM
- GRID RAM
- MINOR SYSTEM PATTERN RAM,
- CONTROL REG. AØH.
- SOUND VOLUME REG: AAH

CANNOT READ ATTRIBUTE OF MINOR SYSTEM

READ ONLY:
- X-REG A5H
- Y-REG A4H
- OVERLAP STATUS REG A2H ~~Control Status~~
- CONTROL STATUS REG A1H

WRITE ONLY:
- MINOR SYSTEM LINEAR STORE (ATTRIBUTE REGS) (ATTRIBUTE OF MINOR SYS.)
- COLOR LATCH A3H
- ENABLE OVERLAP A2H
- SOUND REGS Ø, 1, 2 A7, A8, A9H

The addressable function block structure may be shown by means of an address map as follows:



MINOR SYSTEMS

ADDRESSING

System No.	Y CAM	X CAM	LSS
0	00	01	02
1	04	05	06
2	08	09	0A
3	0C	0D	0E

WORD FORMATS

Bits	7	6	5	4	3	2	1	0
Y CAM	MSB							LSB
X CAM	MSB							2ndLSB
LSS			B	G	R	D	S	X^9

PATTERN RAM Address

System No	Address		
0	80	~~80~~	line 1
		~~81~~	line 2
	87	~~87~~	line 8
1	88	~~90~~	line 1
		~~91~~	line 2
	8F	~~97~~	line 8
2	96	~~A0~~	line 1
		~~A1~~	line 2
		~~A7~~	line 8
3	9F	~~B0~~	line 1
		~~B1~~	line 2
	9F	~~B7~~	line 8

RAM Word Format

Bits	7	6	5	4	3	2	1	0
	last out ←							→ lst out

MAJOR SYSTEMS

ADDRESSING

System No.	Y CAM	X CAM	LSS#1	LSS#2	LSS#3	LSS#4
0	10	11	12,13			
1	14	15	16,17			
2	18	19	1A,1B			
3	1C	1D	1E,1F			
4	20	21	22,23			
5	24	25	26,27			
6	28	29	2A,2B			
7	2C	2D	2E,2F			
8	30	31	32,33			
9	34	35	36,37			
10	38	39	3A,3B			
11	3C	3D	3E,3F			
12	40	41	42,43	46,47	4A,4B	4E,4F
13	50	51	52,53	56,57	5A,5B	5E,5F
14	60	61	62,63	66,67	6A,6B	6E,6F
15	70	71	72,73	76,77	7A,7B	7E,7F

WORD FORMATS

Bits	7	6	5	4	3	2	1	0
Y CAM	MSB						LSB	
X CAM	MSB							LSB
LSS(0-7)	2ndMSB			Displacement				LSB
LSS(8-11					B	G	R	MSB

Displacement = Object Starting Address - Hor. Scan Line Number

CANGIE

MOVABLE PRIMARY OBJECT SYSTEM

4 SYSTEMS

The Primary Object section displ : 4 independently positionable objects each comprised of a dot matrix specified in a loadable 8x8 Pattern Ram, Attribute Regist and Position Register

Each Position Register pair provides 8 bits of vertical position (selecting 1 of 256 lines) and 8 bits of horizontal position (selecting 1 of 256 280 NS positions), and origins the top left corner of the pattern. Additional horizontal accuracy is controlled by two control bits X_8 and Smoothing in the Attribute Regi. Additionaly th Duration bit controls horizontal duration (280NS OR 560 NS) and doubles vertical size also. Control bits BGR provide color selection

DURATION (D)	SMOOTHING (S)	X_8	EVEN LINE DELAY NS	ODD LI DELA
0	0	0	0	0
0	0	1	140	140
0	1	0	140	0
0	1	1	0	140
1	0	0	0	0
1	0	1	280	280
1	1	0	280	0
1	1	1	0	280

4 of EACH

Attribute Register

7		COLOR			SIZE		0
-	-	B	G	R	D	S	X_8

Smoothing

Position Register

	7							0	
X	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	HORIZ.
Y	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0	VERT.

Pattern Ram

	7							0
Row 0	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
⋮								
Row 7	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0

SM
10/30/76

MINOR SYSTEMS

	ADDRESS	DATA BITS 7 6 5 4 3 2 1 0	COMMENTS
(EXAMPLE)	1 6 Ø Ø		VERTICAL POSITION 8-BITS
	1 6 Ø 1		HORIZ POSITION - 9 BITS (9TH IN NXT LOC.)
	1 6 Ø 2	Blue Green Red Dn Sm X9	ATTRIBUTES
	1 6 Ø 3	X X X X X X X X	NOT USED

ADDRESSES SHOWN FOR MINOR SYSTEM #1

16Ø4-7 FOR #2 16Ø8-B FOR #3 16ØC-F FOR #4

VERT. LIMITS 1ØH - DØH

HORIZ. LIMITS ØH - AØH FOR ON-SCREEN LIMITS ON SONY T.V.

MAJOR SYSTEMS

ADDRESS	DATA BITS 7 6 5 4 3 2 1 Ø	
ØØ	*	VERT POS. 7 BITS. LSB NOT USED
Ø1		HORIZ POS. 5 BITS
Ø2		DISPLACEMENT = (VERT. POS. − HORIZ. SCAN LINE #.)
Ø3	Blue Green Red MSB X9	ATTRIBUTES + MSB DISPL.

ROM: object starting address − (Vert. Pos.)/2

SECONDARY OBJECT SYSTEM

The Secondary Object section displays 12 independently positionable objects, each as an 8-dot by 7-line matrix, by selecting one of 45 fixed ROM patterns using a loadable Pointer Register, Color Attribute, and Position Register.

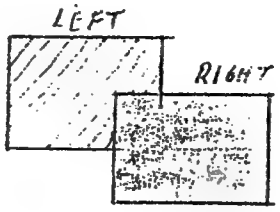
Each Position Register pair provides for 7-bits of vertical position (selecting 1 of 128 even numbered lines), and 8-bits for horizontal location (selecting 1 of 256 280 ns dots) and origins the top left corner of the pattern on the displ

The 9-bit value in the Pointer Register is added to the 7 high order bits of the Vertical Blc* to form a 9-bit effective address which selects one 8 bit row (out of 315) o a 7-line pattern from the fixed pattern ROM. Each ROM bit 1/0 causes a dot/space for 280 ns duration, Care must be exercised so that this effective address selects the first row in the ROM for that Position Register value.

Pointer Register

← 12

Secondary objects must not be positioned so as to overlap more than 4 positions of another secondary object. Any overlap of 4 positions or less will cause the left-most object to be blanked in those positions containing dots or spaces from the right-most object. (Rightmost appears in-front of left object.)



RIGHT OVER LEFT

See also Secondary object overlap detection

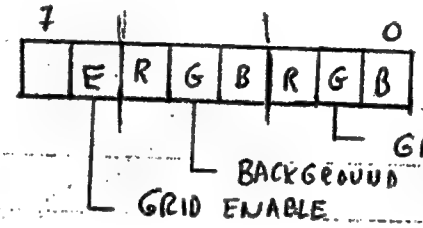
SW
10/30/76

BIT	CONTROL	STATUS	OVERLAP
7	GRID WIDE	SECONDARY OVERLAP	SEC/(PRIM OR GRID)
6	GRID DOT	XTRNAL OVERLAP	XTRNAL CHIP
5	DISPLAY ENABLE	—	HORIZ GRID
4	EXT OVERLAP ENABLE	—	VERT GRID
3	GRID BRIGHT	VERTICAL BLANK ↑	PRIMARY 3
2	SOUND INTRUPT ENABLE	SOUND SERVICE 1	2
1	POSITION STROBE CONTRL	POSITION STROBE ↑	1
0	HORIZ INTRUPT ENABLE	HORIZ BLANK Y	0

DOES NOT EFFECT SOUND

FREEZES X, Y REG IF POS. STROBE LOW

COLOR LATCH



ADDRESS	REGISTER
101 X 0000	CONTROL FRM 8048 TO 8244
0001	STATUS
0010	OVERLAP / OVERLAP ENABLE
0011	COLOR
0100	Y REGISTER
0101	X REGISTER
~~0110~~	~~OVERLAP ENABLE~~
0111	SOUND 0
1000	" 1
1001	" 2
1010	VOLUME (STATUS)

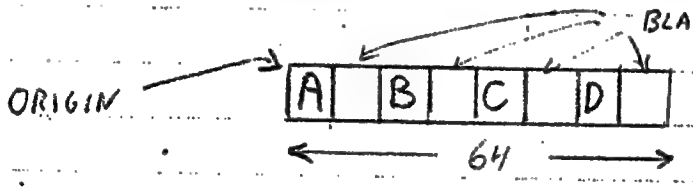
SM 10/30/96

GROUP OBJECT SYSTEM

The Group Object section displays 16 objects in 4 groups of 4 secondary objects. Each group of 4 secondary objects are displayed horizontally spaced 8 dots apart filling a total of 64 dot positions and 4 lines.

Each Position Register origins the top left corner of the first objects pattern. Four Pointer Registers are used for each Group.

Pointer Register	1ST	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	B	G	R	for "A"
	2ND	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0	B	G	R	"B"
	3RD	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0	B	G	R	"C"
	4TH	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	B	G	R	"D"



SM
10/30/76

3211 ADDRESSING

CAM AND LINKER SELECT STORE

ADDRESS			DESCRIPTION
7	6 5 4 3 2	1 0	
0	<OBJECT #>	0 0	LINE CAM
0	<OBJECT #>	0 1	DOT CAM
0	<OBJECT #>	1 0	LSS BITS 0-7
0	<OBJECT #>	1 1	LSS BITS 8-11

system.lin store

MINOR SYSTEM PATTERN RAM

7	6 5	4 3	2 1 0	
1	0 0	CEL #	LINE #	MINOR SYSTEM PATTERN RAM

MISCELLANEOUS REGISTERS.

7	6 5	4	3 2 1 0	
1	0 1	X	0 0 0 0	CONTROL
1	0 1	X	0 0 0 1	CONTROL STATUS
1	0 1	X	0 0 1 0	OVERLAP STATUS
1	0 1	X	0 0 1 1	COLOR LATCH
1	0 1	X	0 1 0 0	Y REGISTER
1	0 1	X	0 1 0 1	X REGISTER
1	0 1	X	0 1 1 0	SOUND 0 ← EN OVERLAP
1	0 1	X	0 1 1 1	SOUND 1
1	0 1	X	1 0 0 0	SOUND 2
1	0 1	X	1 0 0 1	SOUND VOLUME

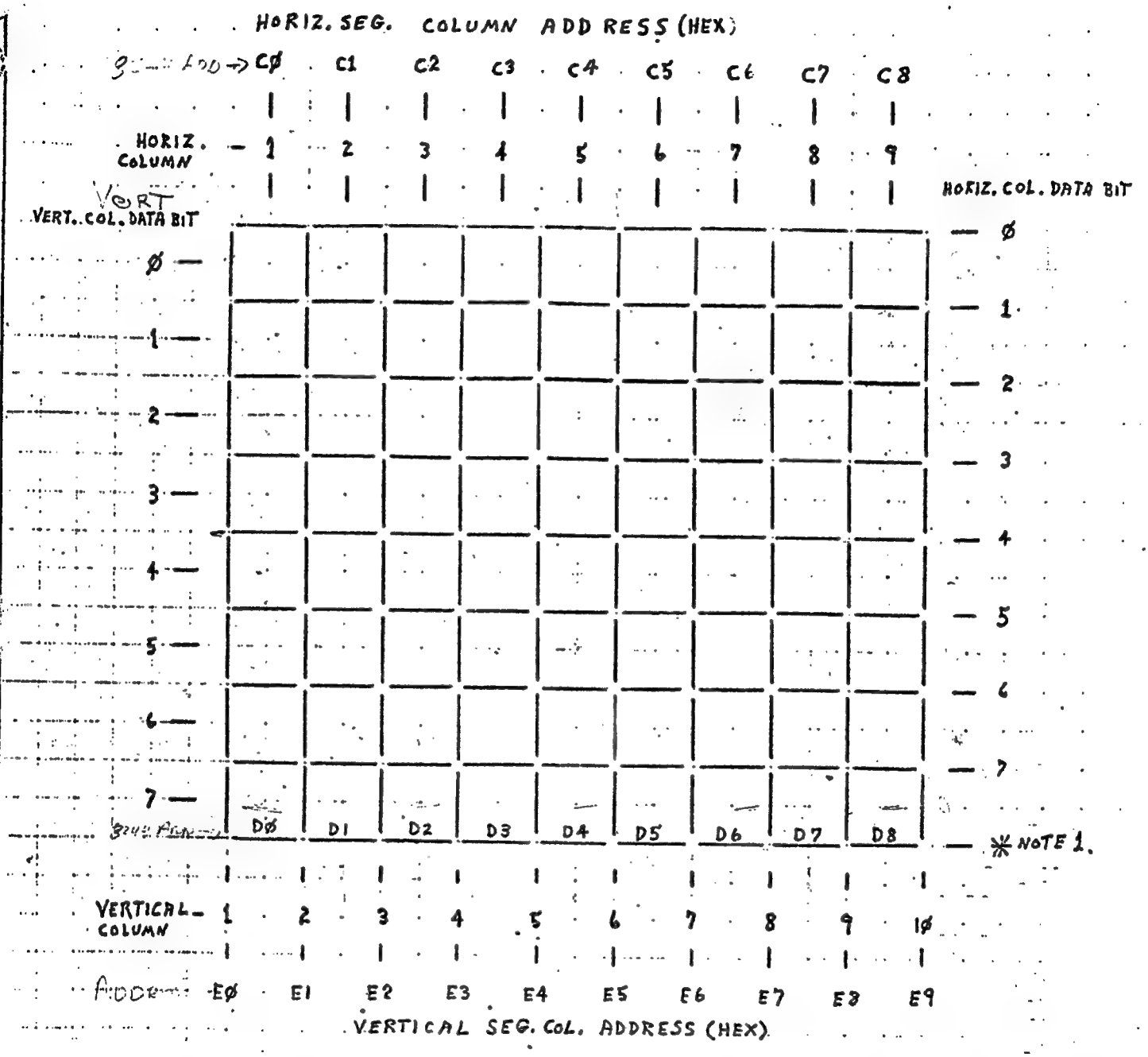
GAID

7 6	5 4 3 2 1	0
1 1	0 COLUMN	0
1 1	0 NUMBER	1
1 1	1	0

PAGE OF

ADDRESS		0	1	2	3	4	5	6	7		8	9	A	B	C	D	E	F
0000	SP	00	00	00	00	00	00	00	00	A	18	66	C3	C3	FF	C3	C3	[illegible]
0010	B	7F	C3	C3	7F	C3	C3	7F	00	C	7E	C3	03	03	03	C3	7E	[illegible]
0020	D	7F	C3	C3	C3	C3	C3	7F	00	E	FF	03	03	3F	03	03	FF	[illegible]
0030	F	FF	03	03	3F	03	03	03	00	G	7E	C3	03	03	E3	C3	FE	[illegible]
0040	H	C3	C3	C3	FF	C3	C3	C3	00	I	3C	18	18	18	18	18	3C	[illegible]
0050	J	C0	C0	C0	C0	C0	C3	7E	00	K	C3	63	33	1F	33	63	C3	[illegible]
0060	L	03	03	03	03	03	03	FF	00	M	C3	E7	FF	DB	C3	C3	C3	[illegible]
0070	N	C3	C7	CF	DB	F3	E3	C3	00	O	7E	C3	C3	C3	C3	C3	7E	[illegible]
0080	P	7F	C3	C3	7F	03	03	03	00	Q	7E	C3	C3	C3	F3	63	DE	[illegible]
0090	R	7F	C3	C3	7F	33	63	C3	00	S	7E	03	03	7E	C0	C3	7E	[illegible]
00A0	T	FF	18	18	18	18	18	18	00	U	C3	C3	C3	C3	C3	C3	7E	[illegible]
00B0	V	C3	C3	C3	C3	66	3C	18	00	W	C3	C3	C3	DB	DB	FE	E7	[illegible]
00C0	X	C3	66	3C	18	3C	66	C3	00	Y	C3	66	3C	18	18	18	18	[illegible]
00D0	Ξ	FF	60	30	18	0C	06	FF	00	@	3C	7E	FF	FF	7E	3C	00	[illegible]
00E0	↑	18	3C	7E	18	18	18	18	00	→	00	20	60	FF	60	20	00	[illegible]
00F0	↓	18	18	18	18	7E	3C	18	00	←	00	04	06	FF	06	04	00	[illegible]
C10	[illegible]	FF	FF	FF	FF	FF	FF	FF	00	▯	0F	0F	0F	0F	0F	0F	0F	[illegible]
0110	[illegible]	38	18	FF	7E	3C	18	66	00	#	66	66	FF	66	FF	66	66	[illegible]
0120	$	18	FE	18	7E	D8	7F	18	00	[illegible]	03	0E	3E	FF	3E	0E	03	[illegible]
0130	←	C0	70	7C	FF	7C	70	C0	00	[illegible]	38	18	3C	7E	FF	18	66	[illegible]
0140	(	1C	06	03	03	03	06	1C	00	)	38	60	C0	C0	C0	60	38	[illegible]
0150	※	C3	66	3C	FF	3C	66	C3	00	+	18	18	18	FF	18	18	18	[illegible]
0160	[illegible]	38	18	FF	3C	3C	66	66	00	−	00	00	00	FF	00	00	00	[illegible]
0170	.	00	00	00	00	00	00	18	00	/	60	60	30	18	0C	06	06	[illegible]
0180	0	7E	E3	F3	DB	CF	C7	7E	00	1	18	1C	18	18	18	18	3C	[illegible]
0190	2	7E	C3	E0	38	0E	03	FF	00	3	7E	C3	C0	7C	C0	C3	7E	[illegible]
01A0	4	63	63	63	FF	60	60	60	00	5	FE	03	03	7E	C0	C3	7E	[illegible]
01B0	6	7E	C3	03	7F	C5	C3	7E	00	7	FF	60	30	18	0C	06	03	[illegible]
01C0	8	7E	C3	C3	7E	C3	C3	7E	00	9	7E	C3	C3	FE	C0	C3	7E	[illegible]
01D0	:	00	00	18	00	00	18	00	00	□	FF	C3	C3	C3	C3	C3	18	[illegible]
01E0	<	30	18	0C	06	0C	18	30	00	=	00	00	FF	00	FF	00	00	[illegible]
01F0	>	0C	18	30	60	30	18	0C	00	?	3C	66	30	18	18	00	18	[illegible]

GRID MAP-8244



NOTE 1: BOTTOM ROW OF HORIZONTAL SEGMENTS HAVE SEPARATE ADDRESSES (HEX) AS WRITTEN ON THE GRID DRAWING. DATA TO TURN THESE SEGMENTS ON IS CONTAINED IN DATA WORD BIT ZERO.

REV. 0 - 1/5/77
REV. 1 - 1/10/77

DRN	W. Mistovich	1/5/77
CKD	D. Bastian	1.7.77
APPR		

intel CORP 3065 BOWERS AVE SANTA CLARA CALIF. 95051

GRID MAP-8244

SIZE	CODE	DRAWING NO
A	GRID	

SCALE — REV 1 SHT. 1 OF 1

ADDR			
18 – 1B	"	"	# 3
1C – 1F	"	"	# 4
20 – 23	"	"	# 5
24 – 27	"	"	# 6
28 – 2B	"	"	# 7
2C – 2F	"	"	# 8
30 – 33	"	"	# 9
34 – 37	"	"	# 10
38 – 3B	"	"	# 11
3C – 3F	"	"	# 12
40 – 43	MAJOR GROUP OBJ.		# 1
44 – 47	"	"	# 2
48 – 4B	"	"	# 3
4C – 4F	"	"	# 4
50 – 53	"	"	# 5
54 – 57	"	"	# 6
58 – 5B	"	"	# 7
5C – 5F	"	"	# 8
60 – 63	"	"	# 9
64 – 67	"	"	# 10
68 – 6B	"	"	# 11
6C – 6F	"	"	# 12
70 – 73	"	"	# 13
74 – 77	"	"	# 14
78 – 7B	"	"	# 15
7C – 7F	"	"	# 16
80 – 87	MINOR SYST.		# 1 PATTERN
88 – 8F	"	"	# 2
90 – 97	"	"	# 3
98 – 9F	"	"	# 4

64 BYTES
0100 0000
7654 3210
64 BYTES
128
159

A7	SOUND 0	
A8	SOUND 1	
A9	SOUND 2	
AA	SOUND CONTROL	
C0	GRID HORIZ SEG. COL.	1
C1	" "	2
C2	" "	3
C3	" "	4
C4	" "	5
C5	" "	6
C6	" "	7
C7	" "	8
C8	" "	9
D0	BOTT. ROW, HOR. SEG.	1
D1	" "	2
D2	" "	3
D3	" "	4
D4	" "	5
D5	" "	6
D6	" "	7
D7	" "	8
D8	" "	9
E0	GRID VERT. SEG. COL.	1
E1		2
E2		3
E3		4
E4		5
E5		6
E6		7
E7		8
E8		9
E9		10

23F

Register	7	6	5	4	3	2	1	0
A1 CONTROL STATUS	MAJOR WITH MAJOR	EXT. CHIP OVERLAP			VERT. STATUS (V.BL.)	SOUND NEEDS SERVICE	POSITION STROBE STAT.	HORIZ. STATUS
A2 OVERLAP STATUS / ENABLE OVERLAP	MAJOR WITH MINOR GRID (OR)	EXTERNAL CHIP	HORIZ. GRID & DOTS	VERT. GRID	MINOR SYST. 3	MINOR SYST. 2	MINOR SYST. 1	MINOR SYST. 0
A4 Y REG.	MSB							LSB
A5 X REG.	MSB							LSB
A3 COLOR LATCH		SET GRID BRIGHT	BACKGROUND R	BACKGROUND G	BACKGROUND B	BACKGND. GRID R	BACKGND. GRID G	BACKGND. GRID B
AA SOUND CONTROL	SOUND ENABLE	RECIRCULATE	SHIFT FREQ. 1=3.9KHz 0=263Hz	NOISE ENABLE	VOLUME MSB			VOLUME LSB

GRI | DC | EN | ENA | EN | ENA | FOR | ENA

STAT. SOUND

MINOR SYSTEMS (EXAMPLE: MINOR SYSTEM #1)

ADDR(H)	7	6	5	4	3	2	1	0	COMMENTS
1600									VERTICAL POSITION, 8 BITS
1601									HORIZ. POS. 9BITS (BITS IN NEXT LOC.)
1602							R	M	X_8 ATTRIBUTES
1603	X	X				X	X	X	NOT USED

MAJOR SYSTEMS (EXAMPLE: MAJOR OBJ. #1)

00 – BLACK
08 – RED
10 – GREEN
20 –
28 –
18 –
30 –

ROGRAM EXAMPLE
R GRI: ERT. COL. SEGMT.

V7	V6	V5	V4	V3	V2	V1	V0
128	64	32	16	8	4	2	1
1	Ø	Ø	Ø	1	Ø	Ø	Ø
Ø	Ø	Ø	Ø	1	Ø	1	Ø
1	1	1	1	Ø	Ø	Ø	Ø
1	Ø	1	Ø	1	Ø	1	Ø
Ø	1	Ø	1	Ø	1	Ø	1

ADDRESS - E0 - - E9 (16E0 . . 16E9) GRID VERT. COL SEGMT.

BINARY WT.

= 88 H DATA BITS IN HEX. DEC. CONVERSION

= ØA H

= F Ø H

= A A H } CHECKERBOARD PATTERN IF EXT. GRID ADDR-A0 IS PROVIDED

= 5 5 H } DATA-Ø8

MEMORY MAP 8244

ADDR.(H)	DATA
Ø0 - Ø3	MINOR SYST. #1 OBJ.
Ø4 - Ø7	MINOR SYST. #2 OBJ.
Ø8 - ØB	MINOR SYST. #3 OBJ.
ØC - ØF	MINOR SYST. #4 OBJ.
10 - 13	MAJOR OBJ. #1
14 - 17	" #2
18 - 1B	" #3
1C - 1F	" #4
20 - 23	" #5
24 - 27	" #6
28 - 2B	" #7
2C - 2F	" #8
30 - 33	" #9
34 - 37	" #10
38 - 3B	" #11
3C - 3F	" #12
40 - 43	MAJOR GROUP OBJ. #1
44 - 47	" +2
	" +3

ADDR.(H	DATA
A0	CONTROL REG.
A1	CONTROL STATUS
A2	OVERLAP REG.
A3	COLOR LATCH
A4	Y REGISTER
A5	X REGISTER
A6	N.A
A7	SOUND Ø
A8	SOUND 1
A9	SOUND 2
AA	SOUND CONTROL
C0	GRID HORIZ SEG. COL 1
C1	" " " 2
C2	" " " 3
C3	" " " 4
C4	" " " 5
C5	" " " 6
C6	" " " 7
C7	" " " 8

DISPLAY MAY BE DONE FOR READING + WRITING; CONTROLLERS BELOW.

ADDR	DATA							
HEX	7	6	5	4	3	2	1	Ø
CONTROL	GRID WIDTH, 1 WIDE	DOT ENABLE	ENABLE DISPLAY	ENABLE EXT. OVERLAP	ENABLE GRID	ENABLE SOUND INTER.	FORCED POS. STROBE	ENABLE HOR. INTER.
A1	7	6	5	4	3	2	1	Ø
CONTROL STATUS	MAJOR WITH MAJOR	EXT. CHIP OVERLAP			VERT. STATUS (V. BL.)	SOUND NEEDS SERVICE	POSITION STROBE STAT	HORIZ. STATUS

NOT USED

60 - 63	"	#9
64 - 67	"	#10
68 - 6B	"	#11
6C - 6F	"	#12
70 - 73	"	#13
74 - 77	"	#14
78 - 7B	"	#15
7C - 7F	"	#16
80 - 87	MINOR SYST. #1 PATTERN	
88 - 8F	" " #2	"
90 - 97	" " #3	"
98 - 9F	" " #4	"

128 159

D5	"	6
D6	"	7
D7	"	8
D8	"	9
E0	GRID VERT. SEG. COL.	1
E1		2
E2		3
E3		4
E4		5
E5		6
E6		7
E7		8
E8		9
E9		10

233

MINOR SYSTEMS (EXAMPLE : MINOR SYSTEM #1)

ADDR(H)	DATA BITS								COMMENTS
	7	6	5	4	3	2	1	0	
1600									VERTICAL POSITION, 8 BITS
1601									HORIZ. POS. 9 BITS (BIT 9 IN NEXT LOC.)
1602			[illegible]			R	M	X_9	ATTRIBUTES
1603	X	X	[illegible]		X	X	X	X	NOT USED

MAJOR SYSTEMS (EXAMPLE : MAJOR OBJ. #1)

ADDR(H)	DATA BITS								
	7	6	5	4	3	2	1	0	
1610								*	VERTICAL POS. LSB NOT USED
1611									HORIZ. POS. 8 BITS
1612									DISPLACEMENT ~~VERT POS [illegible] LINES~~
1613					R_N	G_N	K_N	MSB X_9	ATTRIBUTES, & MSB DISPL.

← MSB OF 255

Displacement = RØM object starting address - (Vert. Pos.)/2

SOUND A7	SOUND A8	SOUND A9	AA	SOUND CONTROL	COLOR LATCH	A3	'X' REG.	A5	'Y' REG	A4	OVERLAY ENABLE
7	7	7	7	SOUND ENABLE		7	MSB	7	MSB	7	MAJOR WITH
6	6	6	6	RECIRCULATE	SET GRID BRIGHT	6		6		6	EXTERN
5	5	5	5	SHIFT FREQ. 1=3.9KHZ 0=363HZ	BACKGROUND R	5		5		5	HORIZ. [illegible]
4	4	4	4	NOISE ENABLE	BACKGROUND G	4		4		4	VERT. [illegible]
3	3	3	3	VOLUME MSB	BACKGROUND B	3		3		3	MINOR
2	2	2	2		BACKGND. GRID R	2		2		2	MINOR
1	1	1	1		BACKGND. GRID G	1		1		1	MINOR
0	0	0	0	VOLUME LSB	BACKGND. GRID B	0	LSB	0	LSB	0	MINOR

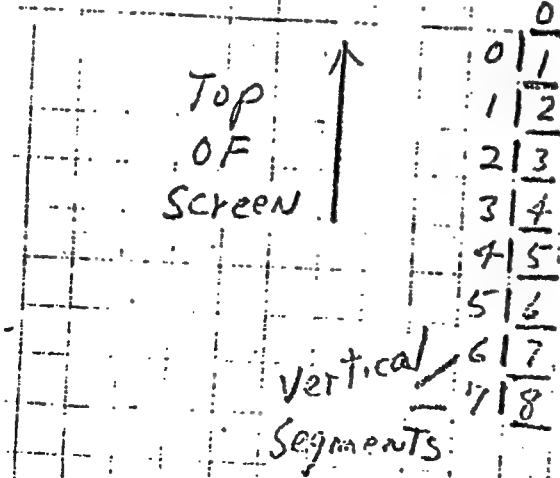
[illegible] LOADS. SEQ

INTERESTING ~~Sound~~ if DISABLE [illegible] AFTER TURNING on 4?H87H A?

GRID

Column Number	Horizontal Segments 0-7 Addresses	Horizontal Segment 8 Address	Vertical Segment Addresses
0	CC 0	C1	EE 0
1	CC 2	C3	EE 2
2	CC 4	C5	EE 4
3	CC 6	C7	EE 6
4	CC 8	C9	EE 8
5	CC A	CB	EE A
6	CC C	CD	EE C
7	CC E	CF	EE E
8	D0	D1	FF 2
9			

Grid Column



Register Address / Bits	Control	Control / Status	Overlap Status / Enable Overlap	Y Register	X Register
	A 0	A 1	A 2	A 4	A 5
7	Grid Width 1=wide	Major with Major	Major with Minor or Grid	MSB	MSB
6	Dot Enable	Ext. Chip Overlap*	External Chip		
5	Enable Display		Horiz Grid		
4	Enable Ext. Overlap		Vert Grid		
3	~~Set Grid Bright~~	Vert. Status (V.B.)	Minor Sys 3		
2	Enable Sound Int.	Sound Needs Service*	Minor Sys 2		
1	Forced Pos Strobe*	Position Strobe Status	Minor Sys 1		
0	Enable Hor. Int.	Horiz. Status*	Minor Sys 0	LSB	LSB

* Explained Below

Forced Position Strobe: Bit = 1 strobes beam location to X-Y registers. Bit = 0 disables strobe. Refer to page 1

External Chip Overlap: Set when an overlap occurs with signal on CX Pin.

Sound Needs Service: Sound register has been shifted out

Position Strobe Status: Ored of Strobe and Forced position Strobe.

Horizontal Status: Starts 20 usec. before leading edge of Horizontal blanking and ends 5 usec before lagging edge of Horizontal blanking.

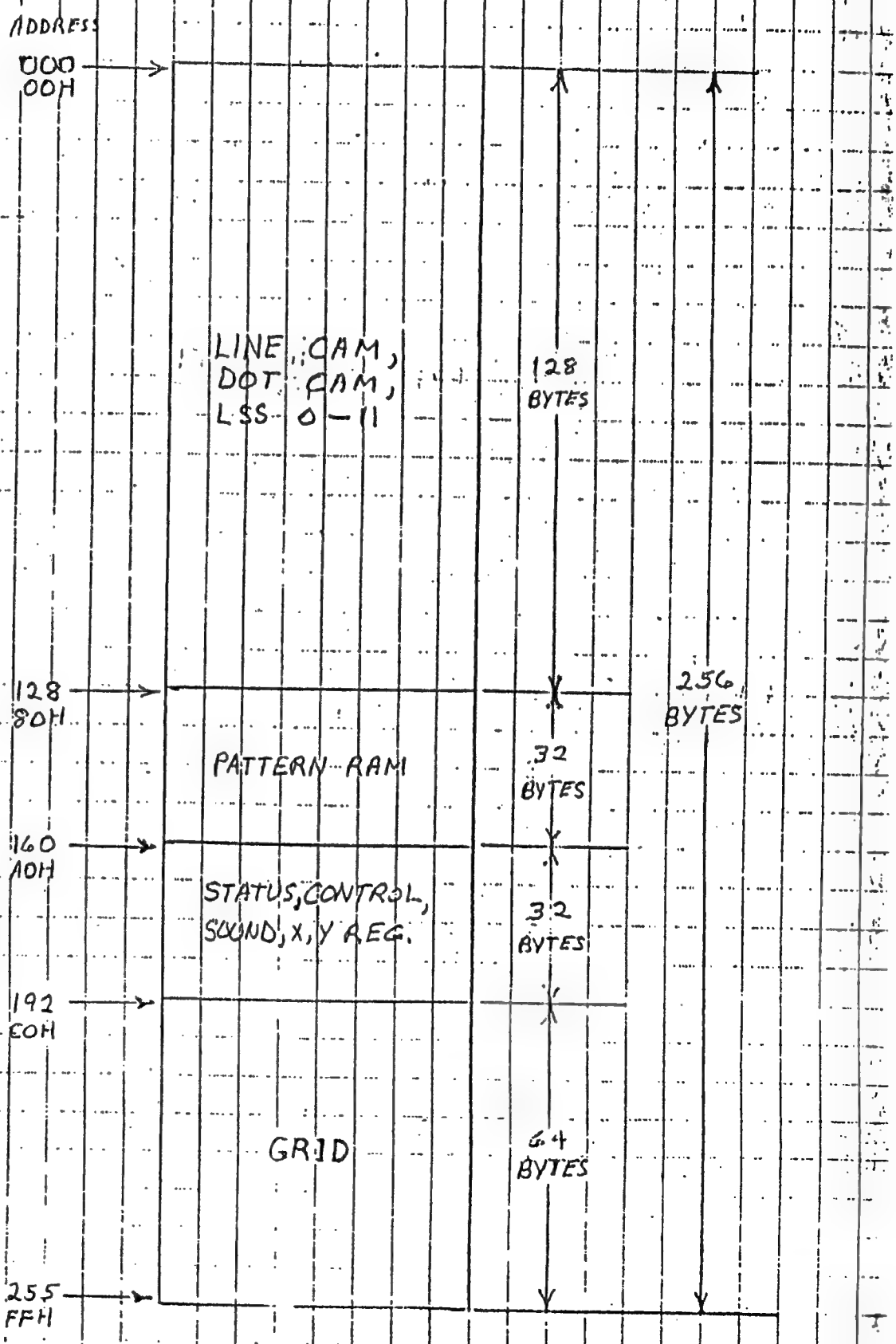
Address	Color Latch W	Sound W 0	Sound W 1	Sound W 2	Sound W Control
7	A3	A7	A8	A9	↓A
6	~~Enable Grid~~ SET GRID BIT	last Bit Out	Last Bit out	Last Bit Out	Sound Enable
5	Background R				Recirculate
4	Background G				Shift Freq.*
3	Background B				Noise Enable
2	Background R				Volume MSB
1	Background G				↑ ↓
0	Background B	1st Bit out	1st Bit out	1st Bit Out	Volume LSB

* 1 = 3933 Hz
  0 = 983 Hz

Sound word 2 is 1st word out

Interrupts will be generated for
- Sound
- Vert. Blanking
- Horiz. Blanking
- Ext. overlap

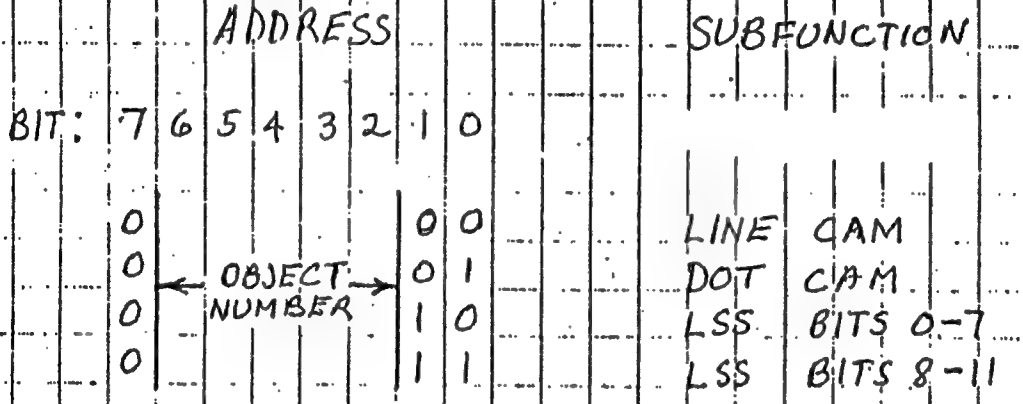
The addressing structure may be shown as an address map as follows:



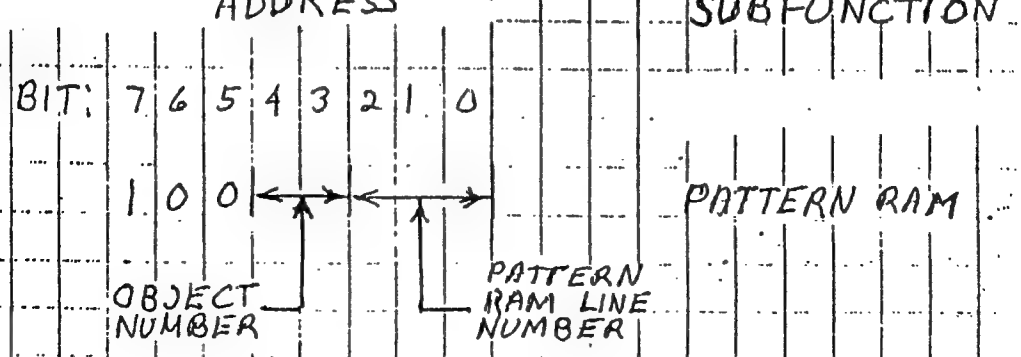
Address Structure

The subfunction blocks within the 8244 may be individually addressed for the writing and, in some cases, the reading of data. The addressing structure of these blocks is shown below:

CAM AND LINEAR SELECT STORE



MINOR SYSTEM PATTERN RAM



CONTROL AND STATUS REGISTERS

BIT	CONTROL*	CONTROL STATUS	OVERLAP STATUS
7	GRID = WIDE SEGMENTS	MAJOR WITH MAJOR *2	MAJOR WITH MINOR OR GRID
6	GRID = DOT	EXTERNAL CHIP OVERLAP	EXTERNAL CHIP
5	ENABLE DISPLAY *1	NA	HORIZ GRID
4	ENABLE EXT OVERLAP	NA	VERT GRID
3	SET GRID BRIGHT	VERT STATUS (VERT BLANK)	MINOR SYSTEM 3
2	ENABLE SOUND INT	SOUND NEEDS SERVICE	MINOR SYSTEM 2
1	FORCED POSITION STB	POSITION STB STATUS	MINOR SYSTEM 1
0	ENABLE HORIZ INT	HORIZ STATUS *3	MINOR SYSTEM 0

* READ/WRITE OTHERS READ ONLY

*1 DISABLES READ/WRITE MUX IN CAM AND LSS AND MINOR SYSTEM RAM AND GRID RAM

*2 BLOCK OVERLAP ALL OTHERS DOT OVERLAP

*3 ADVANCED STATUS.

*NOTE-ALL LATCHES IN STATUS WORDS RESET BY READ OPERATION

CONTROL PIN H→L STORES BEAM LOCATION COUNTER X-Y REGISTER FOLLOWS BLC WHEN CONTROL OR FORCED CONTROL INPUT = 1 STORES WHEN LOW

→ STATUS, CONTROL AND X-Y REGISTERS CAN BE READ OR WRITTEN AT ANY TIME

GRID

11X8

13 CLOCKS/SPACE HORIZONTAL, 2 CLOCKS WIDE, 19 CLOCKS FROM HORIZONTAL RETRACE

24 LINES/SPACE VERTICAL, 3 LINES WIDE, 24 LINES FROM VERTICAL RETRACE

COLOR LATCH (WRITE ONLY)

5	Background	R
4	"	G
3	"	B
2	Grid	R
1	"	G
0	"	B

MISCELLANEOUS REGISTERS

ADDRESS BIT: 7	6	5	4	3	2	1	0	SUBFUNCTION	
1	0	1	X	0	0	0	0	CONTROL	
				0	0	0	1	CONTROL STATUS	(INT)
				0	0	1	0	OVERLAP STATUS	
				0	0	1	1	COLOR LATCH	
				0	1	0	0	Y REGISTER	
				0	1	0	1	X REGISTER	
				0	1	1	0	SOUND 0	A6
				0	1	1	1	SOUND 1	A7
				1	0	0	0	SOUND 2	A8
				1	0	0	1	SOUND VOLUME	A9

GRID

ADDRESS BIT: 7	6	5	4	3	2	1	0	SUBFUNCTION
1	1							

LSS BITS 0-7

7 6 5 4 3 2 1 0

PATTERN # LSB

LSS BITS 8-11

7 6 5 4 3 2 1 0

B G R PATTERN # MSB

LSS MINOR SYSTEM

7	6	5	4	3	2	1	0
B	G	R			DURATION	SMOOTH	X_9

SOUND VOLUME

4 3 2 1 0

NOISE INTENSITY

EN

BIT	CONTROL *	COLOR STATUS	OVERLAP STATUS
7	GRID = WIDE SECTION	MAJOR OVER MAJOR X2	MAJOR WITH MINOR OR GRID
6	GRID = DOT	EXTERNAL CHIP OVERLAP	EXTERNAL CHIP
5	ENABLE DISPLAY	NA	HORIZ GRID
4	ENABLE EXT OVERLAP	NA	VERT GRID
3*	SET GRID BRIGHT	VERT STATUS (VERT BLNK)	MINOR SYSTEM 3
2	ENABLE SOUND INT	SOUND NEEDS SERVICE	MINOR SYSTEM 2
1	FORCED POSITION SIB	POSITION SIB STATUS	MINOR SYSTEM 1
0	ENABLE HORIZ INT	HORIZ STATUS *	MINOR SYSTEM 0

* READ/WRITE OTHERS READ ONLY

*-1 DISABLES READ/WRITE MUX IN CAM AND LSS AND MINOR SYSTEM R.
AND GRID RAM

*2 BLOCK OVERLAP ALL OTHERS DOT OVERLAP

*3 ADVANCED STATUS.

*NOTE-ALL LATCHES IN STATUS WORDS RESET BY READ OPERATION

CONTROL PIN H->L STORES BEAM LOCATION COUNTER X-Y REGISTE
FOLLOWS BLC WHEN CONTROL OR FORCED CONTROL INPUT=1
STORES WHEN LOW

→ STATUS, CONTROL AND X-Y REGISTERS CAN BE READ OR WRITTEN
AT ANY TIME

GRID

9X8

16 CLOCKS / SPACE HORIZONTAL, 2 CLOCKS WIDE, 19 CLOCKS FRO
HORIZONTAL RETRACE

24 LINES / SPACE VERTICAL, 3 LINES WIDE, 24 LINES EACH VE
RETRACE

COLOR LATCH (WRITE ONLY)

5	Background	R
4	"	G
3	"	B
2	Grid	R
1	"	G
0	"	B

7 ~~ENABLE NOISE~~
6 ~~DISABLE~~ DISABLE ENABLE GRID